

**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application.

**LISTING OF CLAIMS:**

1. (Canceled)
2. (Previously presented) The discrete time analog filter according to claim 16, further comprising means for direct sampling, wherein the cascade of single pole IIR filters and means for direct sampling together implement a high order filter devoid of amplifiers.
3. (Original) The discrete time analog filter according to claim 2, wherein the means for direct sampling comprises a multi-tap direct sampling mixer.
4. (Currently amended) A high order~~discrete-time analog~~ filter comprising:  
a cascade of single pole IIR filters configured to generate an output signal in response to an input signal;  
and means for direct sampling coupled to the cascade of single pole IIR filters; and  
at least one amplifier stage coupled to the cascade of single pole IIR filters, ~~wherein the cascade of single pole IIR filters, the means for direct sampling, and the at least one amplifier stage together implement a high order filter.~~

5. (Currently amended) The ~~high order discrete time analog~~ filter according to claim 4, wherein the means for direct sampling comprises a multi-tap direct sampling mixer.

6. (Previously presented) The discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters together implement a high order filter devoid of amplifiers

7. (Previously presented) The discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters is operational to create a uni-directional flow of information, signal, or charge and disallow any feedback from a later filter stage to an earlier filter stage.

8. (Currently amended) The discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters comprises a history capacitor coupled to ~~that is charged together with~~ a first rotating capacitor in a first capacitor bank ~~for a predetermined time period while a charge in a second capacitor bank is charge shared with a buffer capacitor and a second rotating capacitor, and wherein during a subsequent time period, the first capacitor bank holding its charge is charge shared with the buffer capacitor while the second capacitor bank which was charge shared in a previous time period now collects new samples together with the history capacitor.~~

9. (Currently amended) The discrete time analog filter according to claim 8, further comprising a second capacitor bank comprising a buffer capacitor coupled to a second rotating capacitor, the first capacitor bank being coupled to the first capacitor bank wherein the charge on the second rotating capacitor is reset only after it charge shares with

~~the buffer capacitor on the following stage and before it obtains a new sample from the preceding stage.~~

10. (Currently amended) The discrete time analog filter according to claim 16, further comprising:

a comparator responsive to the filter output signal to generate an output signal therefrom;

~~a negative-feedback loop coupling an output of the comparator to an input of enclosing the cascade of single pole IIR filters and the comparator such that the input signal consists of an RF input signal combined with a negative feedback signal flowing in the negative feedback loop.~~

11. (Original) The discrete analog filter according to claim 10, wherein the cascade of single pole IIR filters together operate as a loop filter inside a sigma delta loop.

12. (Original) The discrete analog filter according to claim 10, wherein the input signal consists of an RF input signal minus a negative feedback signal flowing in the negative feedback loop.

13. (Original) The discrete analog filter according to claim 10, wherein the comparator comprises an ADC.

14. (Original) The discrete analog filter according to claim 13, wherein the ADC comprises a multi-bit flash ADC.

15. (Original) The discrete analog filter according to claim 10, wherein the negative feedback loop comprises a digital-to-analog converter (DAC).

16. (Previously presented) A discrete time analog filter comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, wherein the single pole IIR filters are comprised solely of switches and capacitors.

17. (Currently amended) A discrete time analog filter comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, wherein the cascade of single pole IIR filters comprises:

a history capacitor;

a first set of rotating capacitors, wherein at least one ~~a subset of the first set of~~ rotating capacitors is connected to the history capacitor;

a buffer capacitor connected to at least one of the rotating capacitors other than the ~~at least one of the rotating capacitors connected to the history capacitor~~ ~~different subset of the first set of rotating capacitors~~; and

a second set of rotating capacitors, wherein at least one ~~subset of the second set of~~ rotating capacitors is connected to the buffer capacitor.

18. (Currently amended) The discrete time analog filter according to claim 17, wherein after a predetermined period of time, at least one other of the rotating capacitors of the first set of rotating capacitors ~~subset of the first set of rotating capacitors~~ is connected to the history capacitor and at least one other of the rotating capacitors ~~another subset of the second set of rotating capacitors~~ is connected to the buffer capacitor, such that the respective ~~subsets of~~ rotating capacitors connected to the history capacitor and buffer capacitor operate in a ping-pong fashion.

19. (Original) The discrete time analog filter according to claim 17, wherein each set of rotating capacitors consists of two capacitors.

20. (Original) The discrete time analog filter according to claim 17, wherein the first and second set of rotating capacitors are configured as a pair of capacitor banks that operate in a ping-pong fashion with respect to one another.

21-23. (Canceled)

24. (Currently amended) A receiver front-end comprising:  
a cascade of single pole IIR filters configured to generate an output signal in response to an input signal;  
~~and~~ means for direct sampling coupled to the cascade of single pole IIR filters; and  
at least one amplifier stage coupled to the cascade of single pole IIR filters, wherein the cascade of single pole IIR filters, the means for direct sampling, and the at least one amplifier stage together implement a high order filter.

25. (Original) The receiver front-end according to claim 24, wherein the means for direct sampling comprises a multi-tap direct sampling mixer.

26. (Original) The receiver front-end according to claim 21, wherein the cascade of single pole IIR filters together implement a high order filter devoid of amplifiers.

27. (Original) The receiver front-end according to claim 21, wherein the cascade of single pole IIR filters is operational to create a uni-directional flow of information, signal, or charge and disallow any feedback from a later filter stage to an earlier filter stage.

28. (Currently amended) A receiver front-end comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, wherein the cascade of single pole IIR filters comprises a history capacitor coupled to that is charged together with a first rotating capacitor in a first capacitor bank ~~for a predetermined time period while a charge in a second capacitor bank is charge shared with a buffer capacitor and a second rotating capacitor, and wherein during a subsequent time period, the first capacitor bank holding its charge is charge shared with the buffer capacitor while the second capacitor bank which was charge shared in a previous time period now collects new samples together with the history capacitor.~~

29. (Currently amended) The receiver front-end according to claim 28, further comprising a second capacitor bank comprising a buffer capacitor coupled to a second rotating capacitor, the first capacitor bank being coupled to the first capacitor bank wherein the charge on the second rotating capacitor is reset only after it charge shares with the buffer capacitor on the following stage and before it obtains a new sample from the preceding stage.

30. (Currently amended) A receiver front-end comprising:  
a cascade of single pole IIR filters configured to generate an output signal in response to an input signal.

a comparator responsive to the filter output signal to generate an output signal therefrom; and

a ~~negative feedback loop coupling an output of the comparator to an input of~~  
~~enclosing the cascade of single pole IIR filters and the comparator such that the input~~  
~~signal consists of an RF input signal combined with a negative feedback signal flowing in~~  
~~the negative feedback loop.~~

31. (Original) The receiver front-end according to claim 30, wherein the cascade of single pole IIR filters together operate as a loop filter inside a sigma delta loop.

32. (Original) The receiver front-end according to claim 30, wherein the input signal consists of an RF input signal minus a negative feedback signal flowing in the negative feedback loop.

33. (Original) The receiver front-end according to claim 30, wherein the comparator comprises an ADC.

34. (Original) The receiver front-end according to claim 33, wherein the ADC comprises a multi-bit flash ADC.

35. (Original) The receiver front-end according to claim 30, wherein the negative feedback loop comprises a digital-to-analog converter (DAC).

36. (Canceled)

37. (Currently amended) A receiver front end comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal ~~The receiver front end according to claim 21,~~ wherein the cascade of single pole IIR filters comprises:

a history capacitor;

a first set of rotating capacitors, wherein at least one ~~a subset of the first set of~~ rotating capacitors is connected to the history capacitor;

a buffer capacitor connected to at least one of the rotating capacitors other than the at least one of the rotating capacitors connected to the history capacitor ~~different subset of the first set of rotating capacitors;~~ and

a second set of rotating capacitors, wherein at least one ~~subset of the second set of~~ rotating capacitors is connected to the buffer capacitor.

38. (Currently amended) The receiver front-end according to claim 37, wherein after a predetermined period of time, at least one other of the rotating capacitors of the first set of rotating capacitors ~~subset of the first set of rotating capacitors~~ is connected to the history capacitor and at least one other of the rotating capacitors ~~another subset of the second set of rotating capacitors~~ is connected to the buffer capacitor, such that the respective ~~subsets of~~ rotating capacitors connected to the history capacitor and buffer capacitor operate in a ping-pong fashion.

39. (Original) The discrete time analog filter according to claim 37, wherein each set of rotating capacitors consists of two capacitors.

40. (Original) The discrete time analog filter according to claim 37, wherein the first and second set of rotating capacitors are configured as a pair of capacitor banks that operate in a ping-pong fashion with respect to one another.